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May 25, 2006
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No. 2304**
Ryoji YAMAGUCHI et al.	:	Attorney Docket No. 99_0926A
Serial No. 09/380,187	:	Group Art Unit 2616
Filed August 26, 1999	:	Examiner James A. Fletcher
CODED SIGNAL REPRODUCTION APPARATUS	:	**Mail Stop: APPEAL BRIEF-PATENTS**

APPEAL BRIEF

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following is Appellants' Brief, submitted under the provisions of 37 CFR 41.37. Pursuant to the provisions of 37 CFR 41.20, this Brief is submitted with a fee of $500.00. Further, the Brief is accompanied by a Petition and fee for a two month extension of time period set forth in 37 CFR 41.37(a)(1).

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REAL PARTY IN INTEREST

The real party in interest is MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., the assignee of record.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

STATUS OF CLAIMS

Claim 11 has been canceled.

Claims 1-10 and 12-18 stand finally rejected.

The Appellants now appeal the rejection of claims 1-10 and 12-18.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the final Office Action of August 25, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A description of the subject matter of the rejected claims is presented below with reference to the written description and drawings of this application.

The subject matter of independent claim 1 is directed to a coded signal reproduction apparatus having a matching status information outputter M1 and a data formatter M2 (see page 12, line 21 through page 13, line 9; and Fig. 9 (it is noted that Fig. 9 is a block diagram illustrating the conceptual structure of the coded signal reproduction apparatus)). The matching status information outputter M1 includes a start code prefix detection unit 2s3, a start code discrimination unit 2s5, and a start code status hold unit 2s14, and the data formatter M2 includes a formatter unit 2s13 (see page 15, lines 13-18; page 18, lines 1-7; and Fig. 1)

The matching status information outputter M1 is able to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of the packet start code (see page 12, line 25 through page 13, line 3; page 18, lines 12-21; and page 20, lines 4-18). The data formatter is then able to output predetermined data in accordance with the matching status information when

the code is judged not to be a part of the packet start code, wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code (see page 13, lines 3-10; page 15, lines 2-18; page 22, line 17 through page 23, line 4; the Table on page 27; and Figs. 10(a) to 10(e) and 11(a) to 11(d)).

The subject matter of independent claim 8 is directed to a coded signal reproduction apparatus having an end code sequence detector that is able to detect, from code sequences of coded data, a code sequence indicating the end of the coded data (see page 36, line 10-25; and Fig. 1, element 2s5). In addition, the coded signal reproduction apparatus is provided with a formatter that is able to add a predetermined number of pseudo data to the rear of the code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data, when a code sequence indicating the end of the code data is detected by said end code sequence detector (see page 36, line 25 through page 37, line 17; Fig. 1, element 2s13; and Figs. 6(a) a and 6(b)).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 and 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,568,274 to Fujinami et al.

Claims 8, 9 and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,172,989 to Yanagihara et al.

Claims 4, 6, 7, 14, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,568,274 to Fujinami et al. in view of U.S. Patent No. 5,633,686 to Boden

Claims 5 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,568,274 to Fujinami et al. in view of U.S. Patent No. 5,768,265 to Toyohara

ARGUMENT

I. Rejection under 35 U.S.C. 102(b) over U.S. Patent No. 5,568,274 to Fujinami et al. (hereinafter "Fujinami")

Claims 1-3 and 10-13

Independent claim 1 recites the features of a matching status information outputter operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of a packet start code; a formatter operable to output predetermined data in accordance with matching status information, wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code. Appellants submit that Fujinami fails to disclose or suggest such a combination of features.

Fujinami discloses an apparatus for recording multiplexed audio and video signals, wherein the apparatus includes a header separation circuit 22, a switching circuit 23, and a control circuit 24 (see Figs. 2 and 12). The header separation circuit 22 separates pack headers and packet headers from a multiplexed signal, supplies the separated headers to the control circuit 24, and supplies the multiplexed signal to an input terminal G of the switching circuit 23 (see col. 3, lines 9-15).

In Fujinami, the control circuit 24 causes the switching circuit 23 to connect the input terminal G successively to the output terminals H1 and H2 in accordance with a stream ID of the packet header received from the header separation circuit 22 (see col. 3, lines 17-22 and col. 15, lines 29-33). By operating the switching circuit 23 of Fujinami in this manner, the video data and the audio data can be separated from one another, wherein the video data is supplied to the video decoder 25 and the audio data is supplied to the audio decoder 26 (see Figs. 2 and 12; and col. 3, lines 22-25).

In the final Office Action, the Examiner has taken the position that the above-noted feature recited in claim 1 of a status information outputter that is operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of a packet start code is disclosed in Fujinami at col. 3, lines 17-22 (see final Office Action at page 4).

In this regard, as noted by the Examiner in the Office Action, col. 3, lines 17-22 of Fujinami recites the following:

> The control circuit 24 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream ID of the packet header received from the header separation circuit 22.

Thus, it appears as though the Examiner has taken the position that the control circuit 24 of Fujinami corresponds to the "matching status information outputter" and that the control signal that is output by the control circuit 24 (i.e., the signal that is utilized to control the switching circuit 23) corresponds to the "matching status information".

As noted above, however, claim 1 recites that that the "matching status information" is output at a head part of a packet start code. In this regard, Appellants note that while a control signal is output by the control circuit 24 of Fujinami in order to control the switching circuit 23, that such a control signal is not "output at a head part of a packet start code". Accordingly, Appellants submit that the control signal output by the control circuit 24 of Fujinami does not correspond to matching status information that is output at a head part of a packet start code, as recited in claim 1.

In addition, with respect to the above-noted feature recited in claim 1 of a formatter operable to output predetermined data in accordance with matching status information, the Examiner has taken the position that this feature is also disclosed by Fujinami at col. 3, lines 17-22 (see final Office Action at page 4). As noted above, col. 3, lines 17-22 of Fujinami recites the following:

> The control circuit 24 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream ID of the packet header received from the header separation circuit 22.

Thus, the Examiner is apparently taking the position that the control circuit 24 of Fujinami corresponds to the "data formatter" of claim 1, and that the control signal which is output from the control circuit 24 corresponds to the "predetermined data" of claim 1. As noted above, however, the Examiner has also taken the position that the control circuit 24 of Fujinami

corresponds to the "matching status information outputter" of claim 1, and that the control signal that is output from the control circuit 24 corresponds to the "matching status information".

Appellants submit that such a position is clearly improper. For example, as claim 1 indicates that the data formatter outputs predetermined data in accordance with the matching status information, it is clear that the Examiner's reliance on the control circuit 24 of Fujinami as corresponding to both of the "matching status information outputter" and the "data formatter" of claim 1 is incorrect.

In other words, as the control circuit 24 of Fujinami is merely responsible for outputting a signal which controls the switching circuit 23, Appellants submit that the control circuit 24 cannot correspond to both of a matching status information outputter that outputs matching status information and a data formatter that outputs predetermined data in accordance with matching status information.

Moreover, as noted above, claim 1 recites that when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code. Thus, as is clearly evident from claim 1, this predetermined data is the predetermined data that is output from the "data formatter" of claim 1.

As noted above, the Examiner has taken the position that the output of the control circuit 24 of Fujinami corresponds to the "predetermined data" in claim 1. However, in the final Office Action, it is noted that the Examiner has taken an inconsistent position by indicating that "the predetermined data" that is output so as to be positioned at a head part of the data other than a header which follows the next packet start code corresponds to a "signal-type marker" disclosed by Fujinami at col. 8, lines 64-67 (see final Office Action at page 5).

Appellants note that the signal-type marker of Fujinami is a marker that is located adjacent to a signal portion of a predetermined type so as to identify the signal portion of the predetermined type in a multiplexed signal (see col. 8, lines 29-32 and 64-67). Thus, it is clear that the signal-type marker of Fujinami is not a signal that is output by the control circuit 24 of Fujinami to control the switching circuit 23.

Therefore, as the Examiner has taken the position that "the predetermined data" of claim 1 corresponds to two completely different pieces of data in Fujinami, it is clear that the Examiner has taken an inconsistent position in formulating the rejection of claim 1.

In view of the foregoing, Appellants submit that Fujinami does not disclose, suggest or otherwise render obvious the combination of a matching status information outputter operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of a packet start code; a formatter operable to output predetermined data in accordance with matching status information, wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code, as recited in claim 1.

Claims 2, 3 and 10-13 depend from claim 1 and are therefore considered patentable at least by virtue of their dependency.

II. Rejection under 35 U.S.C. 102(b) over U.S. Patent No. 6,172,989 to Yanagihara et al. (hereinafter "Yanagihara")

Claims 8, 9 and 18

Independent claim 8 recites the feature of a formatter operable to add a predetermined number of pseudo data to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data. Appellants submit that the Yanagihara fails to disclose or suggest at least this feature of claim 8.

As explained in Yanagihara, communication of MPEG-PS data is not normally performed by using a digital interface in accordance with IEEE 1394 (see col. 1 lines 17-19 and col. 2, lines 51-55). In order to transmit such data in accordance with IEEE 1394, Yanagihara discloses that a pack forming a unit of MPEG-PS data (which has a length of 2,048 bytes) can be converted into packets that are transmitted in accordance with IEEE 1394 (see col. 3, lines 5-12).

For example, in Yanagihara, the above-noted conversion includes dividing an MPEG-PS data pack of 2,048 bytes into eight groups, each group consisting of 256 bytes as source packets (see col. 13, lines 56-62; Fig. 16(B); and Fig. 17, step S1). After being divided into the eight groups, a 4-byte source packet header is added to the headmost end of each source packet, and 28-byte padding data is added to the hindmost end of each source packet in order to form a 288-byte source packet (see col. 13, line 63 - col. 14, line 3; Fig. 16(B); and Fig. 17, steps S2 and S3).

Next, the 28-byte padding data is moved to a position after the source packet header (see col. 14, lines 4-6; Fig. 16(D); and Fig. 17, step S4). After moving the 18-byte padding data, the 288-byte source packets are divided into eight groups, thereby obtaining 36-byte data blocks (see col. 14, lines 15-17; Fig. 16(E); and Fig. 17, step S5). Lastly, a plurality of packets are formed for transmission, each packet including a predetermined number of the 36-byte data packets (see col. 16, lines; Fig. 16(F); and Fig. 17, step S6).

In the final Office Action, the Examiner takes the position that the above-described conversion process of Yanagihara is performed so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data (see final Office Action at pages 2 and 7). Appellants respectfully disagree.

In particular, Appellants submit that while the above-described method in Yanagihara of dividing an MPEG-PS data pack into packets that can be transmitted according to the IEEE 1394 standard involves the addition of 28-bytes of padding data (as shown in Fig. 16(C)), this 28-byte padding data is not added so as to equalize the bus width of pipeline transfer.

As explained in an illustrative embodiment of the present invention, if the width of a data bus for pipeline transfer is n bytes, when video data of an end part of coded data is positioned at the m-th byte from the bus width boundary, n-m or more pieces of padding data will be added such that the video data of the end part of the coded data can be read by pipeline processing (see the specification at page 36, lines 6-15 and Figs. 6(a), 6(b)).

In contrast to the present invention, in Yanagihara, the padding data is merely added so that data packets can be divided into data blocks having a size (i.e., 36 byte data blocks as shown in Fig. 16(E)) that is necessary to convert the MPEG-PS data pack into packets that conform with IEEE 1394. Thus, while the addition of the padding data in Yanagihara is necessary for the above-noted conversion, the addition of the padding data in Yanagihara is not performed so as to equalize the bus width of a pipeline transfer.

In view of the foregoing, Appellants submit that Yanagihara does not disclose, suggest or otherwise render obvious the feature of a formatter that is operable to add a predetermined number of pseudo data to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data, as recited in claim 8.

Claims 9 and 18 depend from claim 8 are therefore considered patentable at least by virtue of their dependency.

III. Rejection under 35 U.S.C. § 103(a) over Fujinami in view of U.S. Patent No. 5,633,686 to Boden (hereinafter "Boden")

Claims 4, 6, 7, 14, 16 and 17

Appellants note that claims 4, 6, 7, 14, 16 and 17 depend from claim 1. Appellants submit that Boden fails to cure the deficiencies of Fujinami, as discussed above, with respect to claim 1. Accordingly, Appellants submit that claims 4, 6, 7, 14, 16 and 17 are patentable at least by virtue of their dependency.

IV. Rejection under 35 U.S.C. § 103(a) over Fujinami in view of U.S. Patent No. 5,768,265 to Toyohara (hereinafter "Toyohara")

Claims 5 and 15

Appellants note that claims 5 and 15 depend from claim 1. Appellants submit that Toyohara fails to cure the deficiencies of Fujinami, as discussed above, with respect to claim 1. Accordingly, Appellants submit that claims 5 and 15 are patentable at least by virtue of their dependency.

V. Conclusion

For the reasons set forth above, it is submitted that Fujinami does not disclose, suggest or otherwise render obvious all of the features of independent claim 1, and that Yanagihara does not disclose, suggest or otherwise render obvious all of the features of independent claim 8.

Accordingly, as the applied prior art does not teach every limitation set forth in the claims, Appellants submit that independent claims 1 and 8, and all claims that depend therefrom should be considered allowable. See Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In view of the foregoing, Appellants respectfully request that the Examiner's decision to finally reject claims 1-10 and 12-18 be reversed.

Respectfully submitted,

Ryoji YAMAGUCHI et al.

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May 25, 2006

CLAIMS APPENDIX - claims on appeal

1. A coded signal reproduction apparatus comprising:

a matching status information outputter operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of the packet start code; and

a data formatter operable to output predetermined data in accordance with the matching status information when the code is judged not to be a part of the packet start code;

wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code.

2. A coded signal reproduction apparatus as described in Claim 1, wherein said matching status information outputter includes:

a head code detection unit operable to detect the matching status of the head part of the packet start code at every predetermined bit from the input code sequence, and to output matching information at the present point of time; and

a matching status historical information hold unit operable to receive the matching information at the present point of time, and to hold historical information of the matching status of the head code.

3. A coded signal reproduction apparatus as described in Claim 1, wherein said matching status information outputter includes:

a head code detection unit operable to detect the matching status of the head part of the packet start code at every predetermined bit from the input code sequence, and to output matching information at the present point of time; and

a matching status historical information hold unit operable to receive the matching information at the present point of time, and to hold historical information of the matching status of the head code; and

a start code discriminator operable to discriminate the packet start code by using the historical information and a packet start code identifier existing in the latter half part of the packet start code.

4. A coded signal reproduction apparatus as described in Claim 1, wherein said matching status information outputter includes:

a head code detection unit operable to detect the matching status of the head part of the packet start code at every predetermined bit from the input code sequence, and to output matching information at the present point of time; and

a matching status historical information hold unit operable to receive the matching information at the present point of time, and to hold historical information of the matching status of the head code; and

a start code discrimination unit operable to discriminate a hierarchy start code of video data in accordance with the historical information and a video hierarchy identifier of coded video data which exists in a position corresponding to the latter half part of the packet start code.

5. A coded signal reproduction apparatus as described in Claim 1, further comprising:

header analyzer operable to analyze the header of the packet to output reproduction information when the code which is input is coded video data;

wherein said data formatter is operable to insert the reproduction information together with information indicating effectiveness of the reproduction information, in a predetermined position in the coded video data.

6. A coded signal reproduction apparatus as described in Claim 4, wherein said header analyzer includes a header analysis unit operable to analyze the header of the packet and to output the reproduction information, and a reproduction information hold unit operable to hold the reproduction information.

7. A coded signal reproduction apparatus as described in Claim 6, wherein said header analyzer is operable to activate when the start code is identified.

8. A coded signal reproduction apparatus comprising:

an end code sequence detector operable to detect, from code sequences of coded data, a code sequence indicating the end of the coded data; and

a formatter operable to add a predetermined number of pseudo data to the rear of the code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data, when a code sequence indicating the end of the code data is detected by said end code sequence detector.

9. A coded signal reproduction apparatus as described in Claim 8, further comprising:

a specific code sequence inserter operable to insert a specific code sequence in the last packet in a packet sequence before decoding;

wherein said formatter is operable to add a predetermined number of pseudo data to the rear of the specific code sequence.

10. A coded signal reproduction apparatus as described in Claim 1, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

12. A coded signal reproduction apparatus as described in Claim 2, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

13. A coded signal reproduction apparatus as described in Claim 3, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

14. A coded signal reproduction apparatus as described in Claim 4, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

15. A coded signal reproduction apparatus as described in Claim 5, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

16. A coded signal reproduction apparatus as described in Claim 6, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

17. A coded signal reproduction apparatus as described in Claim 7, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

18. A coded signal reproduction apparatus as described in Claim 8, wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None